Fence-Free Etching of Iridium Barrier Having a Steep Taper Angle

Field of the Invention

The present invention relates to processes for etching barrier layers used in ferroelectric devices. More particularly, the present invention relates to a process for the fence-free etching of the bottom electrode barrier layer in a ferroelectric capacitor on plug structure.

Background of the Invention

In prior-art wafers, poly silicon or tungsten plugs (contact plugs) are often used as vertical interconnects between metal lines in multilevel interconnect schemes. In ferroelectric capacitors such contact plugs form a capacitor on plug (COP) structure. The ferroelectric materials in FeRAM (Ferroelectric Random Access Memory) and high K materials in DRAM generally are crystallized at a high temperature (600C or above) in oxygen ambient. A thick barrier against oxygen diffusion is needed to prevent the diffusion of oxygen from a ferroelectric capacitor to the contact plug.

An Ir (Iridium) based barrier is a good material to efficiently block this oxygen diffusion. A typical hardmask used during the etching of this Ir barrier is made from TEOS (Tetraethyl Orthosilicate). Due to the low etching selectivity between Ir and TEOS, the thickness of the barrier is limited by the maximum usable hardmask thickness and the TEOS hardmask needs to be very thick compared to the capacitor stack, resulting in a steep side wall angle prior to etching.

FIGURES 1 - 3 show conventional hardmask etching steps for ferroelectric capacitors.

FIGURE 1 shows a wafer 1 following prior art processing steps. Following deposition of a ferroelectric stack, a top electrode (TE) 6 is covered with a TEOS hardmask 2 which was formed using mask resist strip patterning. The patterning of the top electrode 6 is performed using halogen or CO-based recipe to etch materials such as Iridium, Platinum, Iridium Oxide or various conductive oxide films. A portion of an underlying ferroelectric layer 8 (for example, PZT, SBT, or BLT) might also be etched during this step. A

ferroelectric (FE) capacitor 5 is formed from portions including the top electrode 6, ferroelectric layer 8 and a bottom electrode (BE) 3 as shown in the magnified view in th figure.

A Ti or TiN glue-layer 7 serves to adhere the bottom electrode 3 to the substructure of the FE capacitor 5. The substructure includes a top TEOS layer 15 covering a top nitride layer 9. Between the Ti glue-layer 7 and the bottom electrode 3 can be a barrier layer 17 including materials such as Ir (Iridium), IrO_2 (Iridium Oxide) or other materials for blocking oxygen diffusion from the ferroelectric layer 8 to a poly silicon contact plug 13. The poly silicon contact plug 13 passes through the wafer 1 to form an electrical connection between an active region and the bottom electrode 3.

Another TEOS hardmask 4 is deposited in preparation for a second etching step which patterns the bottom electrode 3. During the second etching step, the ferroelectric layer 8 may be further etched along with the bottom electrode 3. There is a slight over-etch through the top TEOS layer 15 along with any intermediate materials such as the layers of Ir (Iridium) and IrO_2 (Iridium Oxide). FIGURE 2 shows the wafer 1 following this conventional patterning of the bottom electrode 3.

FIGURE 3(a) shows a capacitor cell 300 with the thick hardmask 4 having steeply angled sidewalls 19 which is required due to the low selectivity between the Ir of the barrier layer 17 and the TEOS of the hardmask 4. It is desirable to have a thick Ir layer for blocking oxygen diffusion from the ferroelectric layer 8 to the poly silicon contact plug 13, but this is not easily done because it requires a very thick hardmask 4 with the resulting steeply angled sidewalls 19.

FIGURE 3(b) shows the wafer of FIGURE 3(a) after sputtered controlled etching of the bottom electrode 3 and barrier 17 while using the hardmask 4 for patterning the bottom electrode 3. Due to the steeply angled hardmask sidewalls 19, residues of the etching process or fences 21 remain clinging to the hardmask sidewalls 19. These fences 21 are composed of compounds from the etched materials, such as Ir. They have low density and are unstable. During the anneals, they exhibit volume changes and they show poor adhesion

to the side walls. These fences 21 are particularly detrimental to the following encapsulation processes.

It would be desirable to etch the Ir barrier 17 without the resulting fences 21, but Ir is a noble metal with extremely few volatile compounds for use with plasma etching. To improve the volatility, high temperature etching with a fluorine-based recipe can be employed, but formation of the Ir fences 21 can still not be completely suppressed during this etching. To remove these Ir fences 21 with the high-temperature fluorine etching, a considerable overetch is necessary. During this overetch, the underlying layers such as the glue-layer 7 are attacked. The overetch can also result in capacitor damage.

CO-based chemistries, for example, can be used to etch the Ir barrier 17 resulting in a steep taper angle of the sidewall of the barrier 17 and good hardmask selectivity to allow thicker barrier layers. However, when the barrier 17 is etched to have a steep taper angle, thin Ir fences 21 form on the sidewalls of the TEOS hardmask. Moreover, steep capacitor cells are often desirable and thus the TEOS hardmask will have the steep sidewalls 19. Unfortunately, sputtering does not work well for removing the Ir fences 21 from steep TEOS hardmask sidewalls 19. In order to be able to effectively remove the Ir fences 21 by a physical sputtering mechanism from the sidewalls 19 of the TEOS hardmask, the TEOS hardmask would need a low tapered sidewall angled in the range of 60 degrees or less. It is often desirable to taper the sidewalls 19 of the TEOS hardmask at an angle steeper than 80 degrees and thus a physical sputtering mechanism will not work well for removing the Ir fences 21.

It would be desirable to have a fence-free process for etching a barrier layer of a ferroelectric device. In particular, it would be desirable to etch a steeply tapered barrier layer covered by a steeply angled hardmask without ending up with fences clinging to the sidewalls of the hardmask and barrier layer.

Summary of the Invention

A ferroelectric capacitor has a COP structure. An Iridium barrier layer is between a contact plug and a bottom electrode of the capacitor. The barrier is

etched to have a steep taper whil still producing a fence-free capacitor. In order to remove the fences, etching is performed to pattern the bottom electrode and barrier layer using a fluorine-based recipe resulting in the formation of a first fence clinging to sidewalls of a steep TEOS hardmask cover, the bottom electrode and the barrier layer. Next the remaining barrier layer is again etched using a CO-based recipe. A second fence is formed clinging to and structurally supported by the first fence. At the same time, the CO-based recipe etches away a substantial portion of the first fence to remove the structural support provided to the second fence. The second fence is therefore lifted-off from the sidewalls leaving the sidewalls substantially free of clinging fences. The process results in substantially fence-free sidewalls. The etched barrier layer has a sidewall transition. As a result of the etch using the fluorine-based recipe, the barrier layer has a relatively low taper angle of the sidewalls above the sidewall transition. As a result of the etch using the CO-based recipe, the barrier layer has a relatively steep taper angle below the sidewall transition.

Brief Description of the Figures

Further preferred features of the invention will now be described for the sake of example only with reference to the following figures, in which:

FIGURE 1 shows a wafer 1 following prior art processing steps.

FIGURE 2 shows the wafer 1 following conventional patterning of the bottom electrode and barrier.

FIGURE 3(a) shows a prior-art capacitor cell ready for etching of a bottom electrode and barrier.

FIGURE 3(b) shows the capacitor cell of FIGURE 3(a) after sputtered controlled etching of the bottom electrode and barrier and further illustrates fences clinging to the sidewalls of the hardmask.

FIGURE 4 shows the capacitor cell of FIGURE 3(a) following a first etching step of the present invention in which the barrier is partially etched and a thick first fence is formed.

FIGURE 5 shows the capacitor cell of FIGURE 4 during a second etching step during which the remainder of the barrier is etched and a second fence is formed as the first fence is etched.

FIGURE 6 shows the capacitor cell of FIGURE 4 after the second etching step having substantially no fences and having a barrier etched with a steep taper angle.

FIGURE 7 shows the processing steps of the present invention.

Detailed Description of the Embodiments

The present invention uses a two step etching process to etch the Ir barrier layer 17 of the capacitor cell 300 of FIGURE 3A. FIGURE 7 illustrates the steps of the method of the present invention. The method involves two general steps. At a step 701 a fluorine-based recipe (CF4, SF6) 301 plasma etching process is used to partially etch the Ir barrier layer 17 (see FIGURE 3A). At a step 703 a further plasma etching step is performed using a CO-based etching recipe 403 (see FIGURES 4 and 5). The CO-based etching recipe can be CO, Cl_2, N_2, O_2 or CO_1NH_3, for example.

FIGURE 4 shows the capacitor cell 300 following the etching step 701. Typically, about 30% to 90% of the total Ir barrier 17 thickness is removed. During this step thick first fences 401 form. The Ir barrier layer 17 is tapered under the first fence 401, because the fence acts like a gradually widening hardmask. The first fence 401 is rich in Ir, but has a relatively porous structure, and can therefore be removed by a process such as wet chemistry.

FIGURE 5 shows the capacitor cell 300 during plasma etching using the CO-based etching recipe 403 of the step 703. The remaining Ir barrier layer 17 is etched to form an almost vertical taper angle 501, thereby forming a sidewall transition 505. The barrier layer 17 changes from a relatively low taper angle above the sidewall transition 505 to a steep, almost vertical, taper angle below

the sidewall transition 505. During the etching of step 703, because the barrier layer 17 is etched to have a steep taper angle, thin second fences 503, like the fences 21 of FIGURE 3B, form on top of the already existing fences 401. The second fences 503 have a much more compact structure than the fences 401 and cannot be easily removed by wet chemistry.

However, the present invention takes advantage of the second fences 503 being supported by the first fences 401 to remove the second fence 503 while still allowing a steep taper angle of the barrier layer 17. The CO-based etching recipe 403 etches the TEOS hardmask 4 at a low etch rate. Therefore it can be applied to the capacitor cell 300 for a relatively long amount of time. As the CO-based etching recipe 403 etches away the barrier layer 17 and forms the second fences 503, it also etches away the relatively porous first fences 401. Because the second fences 503 are supported by the underlying first fence 401, as the first fence 401 is removed, the fences 503 are also cut off from the sidewalls by a lift-off process. Thus, even though the CO-based etching recipe 403 can not etch away the second fences 503 directly, it can etch away the first fences 401 formed by the fluorine-based recipe 301 of the step 701 to thereby remove the second fences 503.

FIGURE 6 shows the capacitor cell 300 following the etching step 703. The fences 401, 503 are removed. The sidewall of the barrier layer includes an upper area with a lower taper angle 601 (from using the a fluorine-based recipe 301) and an upper area with a steeper taper angle 603 (from using the CO-based etching recipe 403). Therefore the barrier layer 17 is etched to have a steep average taper angle. The capacitor cell 300 can be over-etched into the top TEOS layer 15 using the method of the present invention. The advantages of the CO-based recipe 403 (steep taper angle, good uniformity and high selectivity) are therefore combined with the advantages of the fluorine-based recipe 301 (high etch rate). Time is saved by the present invention because the fast fluorine-based recipe 301 is combined with a relatively slow CO-based recipe.

Other materials can be used for either the barrier layer 17 or the hardmask 4 (for example, the hardmask can be Al_2O_3, TiN or TiAlN used with

barriers formed from Ir or IrO_2) so long as an etching process can be used to etch a first underlying fence while a second overlying fence is formed.

Still other materials and method steps can be added or substitut d for those above. Thus, although the invention has been described above using particular embodiments, many variations are possible within the scope of the claims, as will be clear to a skilled reader.